Simulation of a Micromachined Electro-Mechanically Tunable Capacitor

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Abstract -- A micromachined electro-mechanically-tunable capacitor with two parallel plates has been designed. The tunable capacitor is a modification of the two-plate capacitor as suggested by A. Dec and K. Suyama [1]. Instead of using strip lines to feed the structure, a CPW line was used. Simulations with different feed structures to the suspended plate and air gap sizes are presented. It was shown that the CPW feed doesn't improve the performance, but also doesn't make it worse.

Index Terms -- MEMS, tunable capacitor

I. Introduction

Resonant devices with a high Q-factor are highly demanded in the modern wireless communication. This is because the phase noise is proportional to $1/Q^2$, where Q is the overall Q factor of the resonator [1]. A tunable MEMS capacitor and an inductor integrated on the same chip can provide a high-Q resonant device. This is because the length of the electric connections can be kept small.

Micromachined electro-mechanical structures have shown that there are numerous applications where they can be superior to conventional devices. The integration of a MEMS capacitor has the advantage, that this tunable device can be integrated together with other devices on one silicon chip. This allows integrating an oscillator on a single device. Up to now an external varactor had to be used. As this device can't be implemented together with other circuitry, because it needs a different process to be manufactured. The electro-mechanical tunability of the capacitor makes it an ideal device in the fields of modern communication systems, RF filters, voltage controlled oscillators etc. The purpose of this redesign is to introduce a CPW feed structure, to increase the capacitance tuning ratio by reducing the effect of parasitic inductance and capacitance and to get a higher Q factor. The design issues include the construction of a CPW feed, the rearrangement of mechanical components to allow the extension of the feed structure of the suspended plate from two beams to four wider beams. This is to reduce the parasitic inductance of the feed structure.

II. Background

Let's discuss the original device as shown in Figure II-1 and Figure II-2 [1].

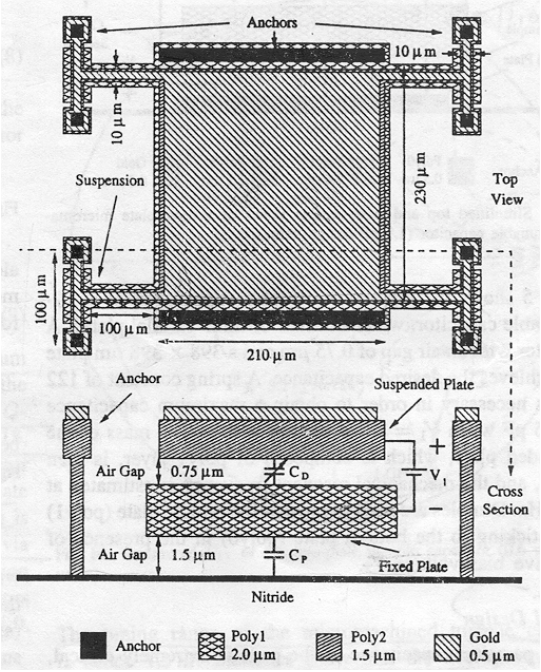


Figure II-1 Schematic view of the original device [1]

Authors are working on ECEN5004 projects, they are graduate students in EM fields at the University of Colorado at Boulder

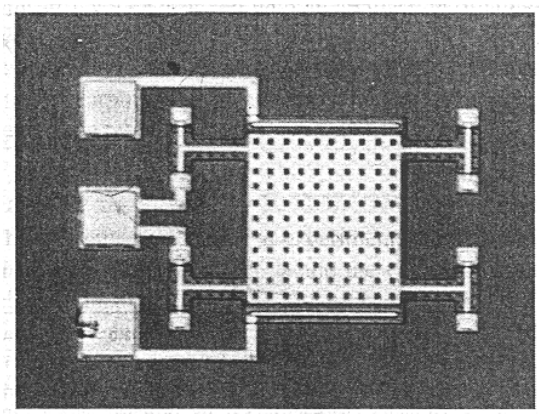


Figure II-2 Photo from top of the original device [1]

The three bonding pads on the left side (Figure II-2) of the device provide a CPW style interface to connect the capacitor to external circuitry. But inside the device feed lines continue as strip lines.

The ground traces (top and bottom, see Figure II-2) provide a stable ground to the fixed lower capacitor plate (Figure II-1). Two wide anchors incorporate the connection from the traces on the nitride to the actual capacitor plate over the whole width of the plate. These wide anchors provide a low inductance connection. The lower plate is elevated from the nitride to reduce parasitic capacitance.

The middle of the three pads is carrying the signal provided to the capacitor. Here we find a problem of the original design. The signal has to propagate over two narrow traces, up the narrow vias, over the narrow suspended traces which work as springs and finally onto the upper capacitor plate. This rather long, narrow path introduces a lot of parasitic inductance. A goal of the redesign is to reduce this parasitic inductance.

Let's discuss the term 'tuning ratio'. The tuning ratio is the highest capacitance to the lowest achievable capacitance of the capacitor. This is of interest, as a voltage-controlled oscillator (VCO) built with this tunable capacitor will have a frequency-tuning ratio equal to the capacitance-tuning ratio. If we want to cover a wide range of frequencies, we need a capacitor with a large tuning ratio.

What can we expect from our capacitor? With equation (II-1) we can evaluate the theoretical capacitance of our capacitor.

$$C = \frac{\varepsilon \cdot A}{d} \qquad \textbf{(II-1)}$$

The maximum and minimum distances are 0.75µm and 0.5µm. The maximum is given by the construction of the MEMS device and the minimum is a structural limit. Now we can calculate the minimum and maximum capacitance

$$C_{\min} = \frac{8.854 \cdot 10^{-12} \cdot 230 \cdot 10^{-6} \cdot 210 \cdot 10^{-6}}{0.75 \cdot 10 - 6} = 0.570\,pF \qquad \textbf{(II-2)}$$

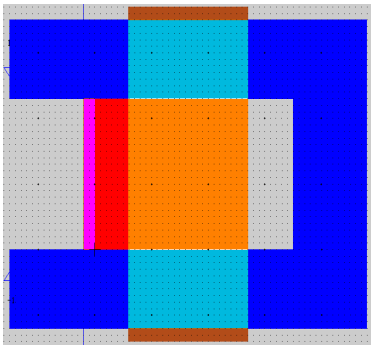
$$C_{\max} = \frac{8.854 \cdot 10^{-12} \cdot 230 \cdot 10^{-6} \cdot 210 \cdot 10^{-6}}{0.5 \cdot 10 - 6} = 0.855\,pF \qquad \textbf{(II-3)}$$

Where we used the area of the 210µm by 230µm suspended plate. The simulated capacitance can vary from these values due to fringing fields (this parasitic capacitance is also tuning and does not influence the tuning ratio) which can enlarge the actual area, due to parasitic capacitance (this capacitance is constant and reduces the tuning ratio) and parasitic inductance (constant) which is reducing the capacitance. With (II-2) and (II-3) we can calculate the theoretic tuning ratio

$$Ratio = \frac{0.855\,pF}{0.570\,pF} = 1.5 \qquad \textbf{(II-4)}$$

III. DESIGN

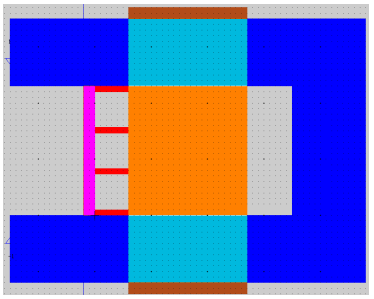
The goal of the redesign is to introduce a CPW feed structure and to reduce the parasitic inductance. The approach is to provide a low inductance connection to the upper capacitor plate. By rotating the upper plate (Figure III-1), including the suspension (not shown in Figure III-1), by 90 degree, we get the vias and the suspension out of the way. Now we have free space on the left and right of the capacitor plates to invent a new method of connecting the suspended capacitor plate. If we go back to the original design, we remember that there have been three critical points. These are the narrow traces, the slim vias and the narrow signal path through the suspension. Introducing the CPW feed line, which gives a wide trace for the signal, solves the first problem. The second is easily solved by introducing a via over the whole with of the capacitor plate, as we used for the lower plate. The signal path from the via onto the capacitor plate is more of a problem. The suggestion is to use several thin connections on the gold layer. These connections introduce little parasitic inductance. These traces might disturb the mechanical behavior of the suspended upper plate. Regarding the low rigidity of gold, the distortions should be of a minor effect. To get a feeling of the effect from the beams connecting the via to the suspended plate, different designs have been simulated. First a one port model was used, which has only one solid connection over the whole width from the via to the suspended plate as shown in Figure III-1. Second a one port model with four connecting beams from the via to the suspended plate as shown in Figure III-2 was used. Third a two port model with solid connections and fourth a two port model with four connecting beams was used (see Figure III-3 and Figure III-4).



Top Layer:
orange/red
Middle Layer:
light blue
Lower layer*
blue
Via Top-Lower:
Cyan
Via Middle-Lower:
Mauve
* Slot layer

Figure III-1 Top view of one port, solid beam capacitor

Figure III-1 is a simplified model for the four beam feed line, which is expected to give similar results as the four beam feed line.



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Via Middle-Lower:
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Figure III-2 Top view of one port, four-beam capacitor

Figure III-2 shows the capacitor as it actually would be implemented.

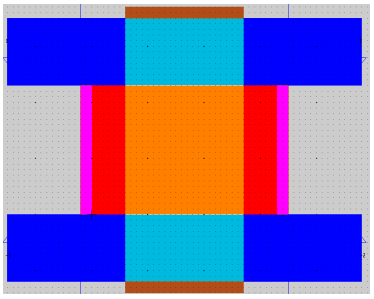

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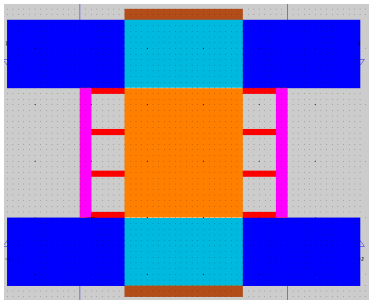
Figure III-3 Top view of two port, solid beam capacitor

Figure III-3 shows an alternative model of the simplified solid connection capacitor. It is a two port design, which can be of an advantage in certain designs where the capacitor should be connected in parallel to a CPW transmission line.



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* Slot layer

Figure III-4 Top view of two port, four-beam capacitor

Figure III-4 shows the alternative two port capacitor with four connection beams as it actually would be implemented.

IV. RESULTS

A. Simulation of one port model

The simulations where done in HP Momentum.

In the actual system the air gap between the plates of the MEMS tunable capacitor can be adjusted continuously to get different values of capacitance. This is performed by providing a DC voltage to the plates. The electrostatic force is then pulling the two plates together, reducing the air gap and increasing the capacitance. We chose the smallest and largest air gap size to model the MEMS tunable structure in our simulations. The initial mechanical distance between the plates is 0.75µm. By applying a DC bias voltage the two plates can move closer to each other. The minimum distance is 0.5µm. This is near the physical limitation of the air gap between the two plates, because the two plates typically will warp during or after the production.

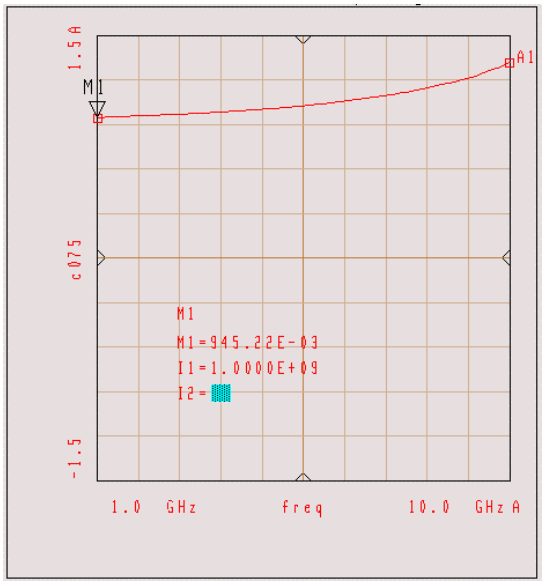

Figure IV-1 One port model, solid beam, air gap is 0.75µm

Figure IV-1 shows the results of the simulation of the one port model with a solid beam and a 0.75µm air gap. This simulation shows that the equivalent capacitance is about 0.945pF at 1GHz.

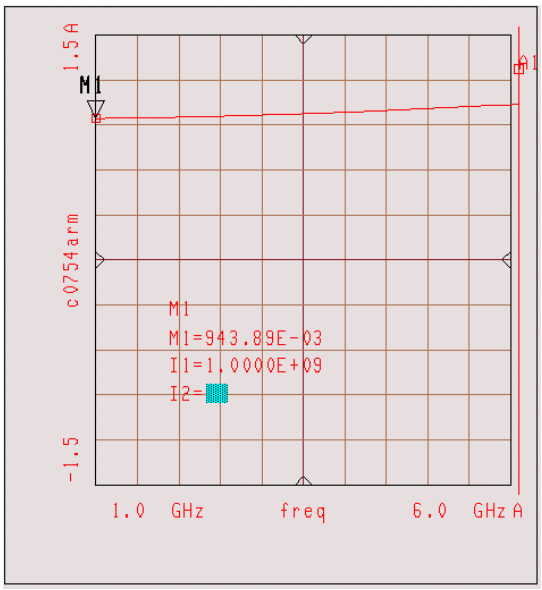

Figure IV-2 One port model, for beams, air gap is 0.75µm

Figure IV-2 shows the simulation result of the same structure as the previous one but with four feeding beams, which actually would be fabricated considering the mechanical issues. This simulation shows the equivalent capacitance is about 0.944pF at 1GHz, which is very close to the one with the solid feeding beam. Consequently, using the model with the solid feeding beam for the simulations can greatly reduce the simulation time and still produce accurate results.

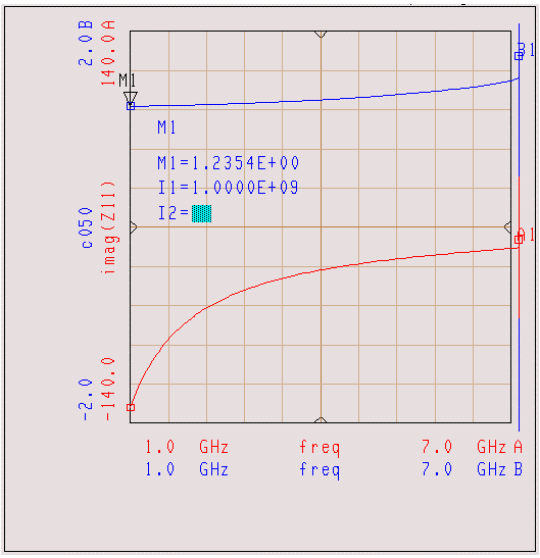

Figure IV-3 One port model, solid beam, air gap is 0.5µm

Figure IV-3 shows the simulation result of the one port model with one solid beam and an air gap of 0.5µm. It shows, that we have a capacitance of 1.24pF at 1GHz. If we compare this with the 0.944pF at 1GHz from Figure IV-1 we get a tuning ratio of

$$\frac{1.24}{0.945}=1.31 \qquad \textit{(IV-1)}$$

This tuning ratio compared to the theoretical one shown in (II-4) is rather small. But if we look at the capacitances calculated and the capacitances simulated we see, that we have about 0.4pF constant parasitic capacitance, which reduces the tuning ratio (see Table IV-1).

Table IV-1 Comparison of parameters of one port models

	Theory	Simulated	Difference
Min. cap.	0.57pF	0.944pF	0.374pF
Max. cap.	0.855	1.24pF	0.385pF
Tuning ratio	1.5	1.31	-0.19

B. Simulation of two port model

Figure IV-4 and Figure IV-5 show the simulation results of the two port capacitor with 0.5µm distance between the plates. Again, we simulate both, solid feeding trace case and four feeding traces. The simulation result from the solid feeding line (Figure IV-4) shows the equivalent capacitance is about 0.615pF at 1GHz. The result for the model with four feeding traces (Figure IV-5) is 0.587pF at 1GHz. These two results are not that close to each other as it was with the one port model. Therefore we will proceed with the simulation results from the four beam simulations.

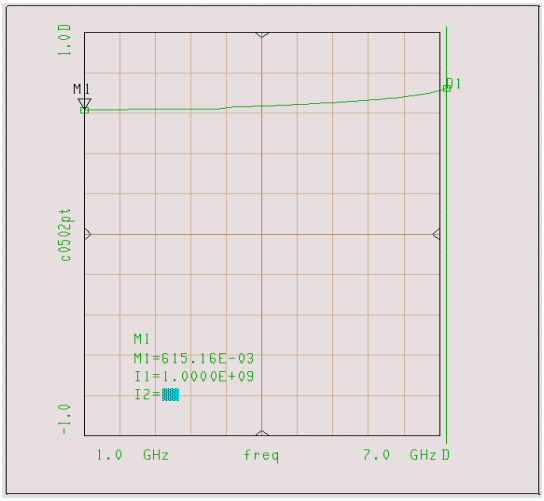

Figure IV-4 Two port model, solid beam, air gap is 0.5µm

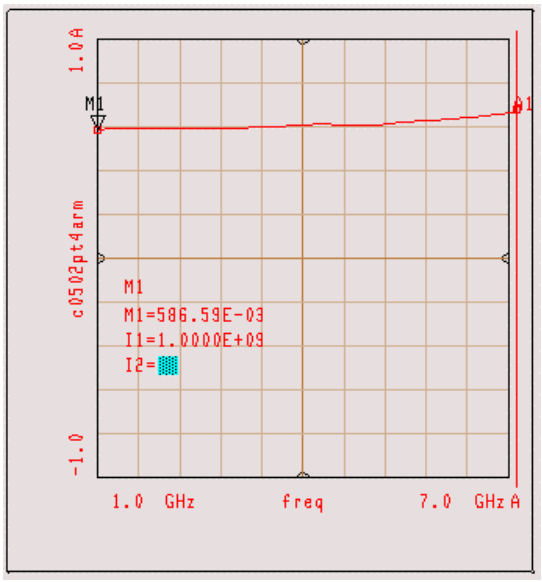

Figure IV-5 Two port model, four beam, air gap is 0.5μm

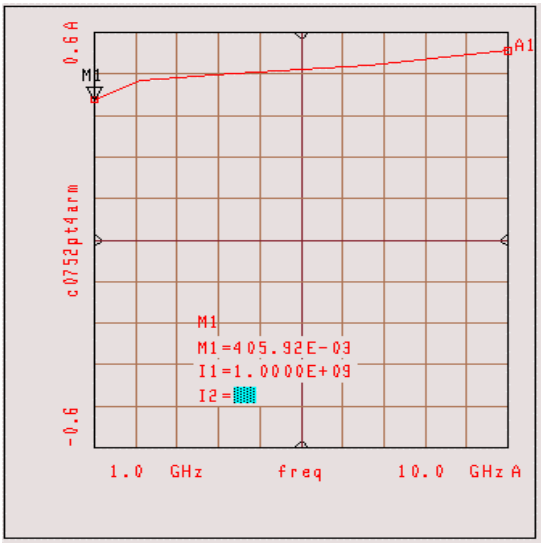

Figure IV-6 Two port model, four beam, air gap is 0.75μm

In Figure IV-6 we see the simulation of the two port model with four feeding lines and a distance between the capacitor plates of 0.75μm. We see that the capacitance is 0.406pF at 1GHz. With this result and the result from Figure IV-4 we can calculate the tuning ratio of the two port capacitor

$$\frac{0.615}{0.406}=1.51 \qquad \textit{(IV-2)}$$

This is even over the theoretical possible tuning ratio calculated in (II-4). This is due to small errors in simulation, which can source from different meshes on the very close layers of the capacitor structure.

Table IV-2 Comparison of parameters of two port models

	Theory	Simulated	Difference
Min. cap.	0.57pF	0.406pF	-0.164pF
Max. cap.	0.855	0.615pF	-0.240pF
Tuning ratio	1.5	1.51	+0.01

C. Comparison of Parameters

	Initial Design	Modified design
Size of plate	230*210μm	230*210μm
Connecting beams	100*10 x 2	80*10 x 4
Gold layer	0.5μm	PEC* thick=0
Substrate circuit	MSTRIP	CPW
Tuning	1.5:1	1.31:1 (one port) 1.51:1 (two ports)
Simulation Capacitance	2.05 PF	1.235 PF(one port) 0.615PF(two ports)
Q factor	20 at 1G Hz	N/A because PEC*

* PEC: Perfect Electric Conductor

V. CONCLUSIONS

If the device, as we suggest it is mechanically feasible, then the performance of the actual physical capacitor would be very good.

The four connecting beams to the upper plate of the one port capacitor may cause some mechanical unbalance due to the fact that the other side of the upper plate is mechanically not connected by any suspension arm nor signal trace. Our result shows the improved design is electrically feasible. The tunable ratio is approaching the theoretical limit.

The CPW MEMS tunable capacitor should provide a higher Q factor due to wider connections and a larger tunable ratio. The simulation results match well with theory and the reference papers.

A model of the original design was also simulated as a comparison of our modified design. Instead of four short connection traces, two long thin traces were connected to the upper capacitor plate in order to model the original design [2]. However, the results could not be used as constantly mismatches happened during the mash generation of HP momentum simulation process for this model.

During the simulation process we experienced different problems with unwanted large tunable inductance, due to the slot layer for the CPW line. We also had to resolve various mesh mismatch problems, which prevented the simulation solver from delivering usable results.

VI. ACKNOWLEDGEMENTS

The authors would like to express their gratitude to Dr. Zhiping Feng and Professor Piket-May for their helpful suggestions and comments.

VII. REFERENCES

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[2] A. Dec and K. Suyama, "Micromachined variable with wide tuning range," Electronic Letters 22nd May 1997 Vol. 33 No.11, pp. 922-924.

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